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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR		ATTORNEY DOCKET NO.
09/164,216	09/30/98	PASQUALINI	R	NSC1-D8400

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MARK C. PICKERING
LIMBACH & LIMBACH
2001 FERRY BUILDING
SAN FRANCISCO CA 94111

EXAMINER	
NADAV,O	
ART UNIT	**PAPER NUMBER**
2811	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No. 09/164,216	Applicant(s) Pasqualini
	Examiner ORI NADAV	Group Art Unit 2811

☒ Responsive to communication(s) filed on *Aug 17, 2000*.

☒ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire *3* month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claims

☒ Claim(s) *1, 5, 6, 10, 11, 15, 17-23, and 32-36* is/are pending in the application.

Of the above, claim(s) _____ is/are withdrawn from consideration.

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) *1, 5, 6, 10, 11, 15, 17-23, and 32-36* is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐approved ☐disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____.

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____.

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☒ Notice of References Cited, PTO-892

☐ Information Disclosure Statement(s), PTO-1449, Paper No(s). _____

☐ Interview Summary, PTO-413

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

--- SEE OFFICE ACTION ON THE FOLLOWING PAGES ---

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 1 and 18 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Claims 1 and 18 recite a well, a second region of a second conductivity type being formed in the well, wherein the second region encircles that particular well. There is no support in the specification for a second region of a second conductivity type encircling a well of a second conductivity type, as recited in claims 1 and 18.

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 11, 21 and 34 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter

which applicant regards as the invention. It is unclear how a third region can be formed in a first region, and yet to encircle the first region, as recited in claims 11 and 21.

5. Claim 34 recites the limitation "the ESD switches" in line 1. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1 and 5, insofar as in compliance with 35 U.S.C. 112, are rejected under 35 U.S.C. 103(a) as being unpatentable over Gens et al. (5,515,225) in view of Rao et al. (5,770,886).

Gens et al. teach in figure 2 a semiconductor chip having a substrate (figure 4, the external line encircling R1) of a first conductivity type, the chip comprising: a pad P2, an ESD positive line R1 not being connected to a voltage source, an ESD negative ring R2, and a plurality of floating lateral clamp diodes (column 3, lines 48-49) connected to

the pad so that first and second floating lateral clamp diodes are connected to the pad and the positive and negative lines, respectively.

Although Gens et al. do not explicitly disclose a positive line R1 not being connected to a voltage source, it is clear from figure 2 and since R1 is floating that positive line R1 is not connected to a voltage source.

Gens et al. do not teach the structure of the floating diode.

Rao et al. teach in figure 2 a diode 11 formed in a well of a second conductivity type 26, wherein plurality of spaced apart first regions of the first conductivity type 35, 36 being electrically connected together, and a second region of the second conductivity type 42 being formed in the well and having dopant concentration higher than that of the well. Rao et al. further teach in figures 3 and 9 a second region of a second conductivity type 40 and 108 encircle the wells 26 and 111, respectively, and having a dopant concentration greater than that of the well.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form the floating diodes of Gens et al. in a circular second region within a double well, as taught by Rao et al., because it is well known in the art to form floating devices including diodes in a double well configuration in order to provide better electrical isolation to the devices.

8. Claims 10-11, insofar as in compliance with 35 U.S.C. 112, are rejected under 35 U.S.C. 103(a) as being unpatentable over Gens et al. in view of Rao et al.
Gens et al. teach in figure 2 substantially the entire claimed structure, as applied to claim 1 above, except the structure of the floating diode.
Rao et al. teach in figure 2 a diode 11 formed in a well of a second conductivity type 26, a plurality of spaced apart second regions of the first conductivity type 35, 36 being electrically connected together, and a third region of the second conductivity type 40, 42 being formed in the well and having dopant concentration higher than that of the well, wherein the third region encircles the first region (figure 3). Rao et al. further teach in figure 9 a first region of a second conductivity type 111 being formed in the well 108, and having a dopant concentration that is less than that of the well.
It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form the floating diodes of Gens et al. in a circular third region within a double well, as taught by Rao et al., because it is well known in the art to form floating devices including diodes in a double well configuration in order to provide better electrical isolation to the devices.

Regarding claim 5, Gens et al. teach in figure 4 a negative line encircling the periphery of the chip.

Regarding claims 12-13, Gens et al. teach floating ESD positive and negative rings connected package pins (column 2, line 43).

9. Claims 6, 15, 19, 22-23 and 32-36 insofar as in compliance with 35 U.S.C. 112, are rejected under 35 U.S.C. 103(a) as being unpatentable over Gens et al. in view of Bass Jr. et al. (6,086,627) and Admitted Prior Art (APA).

Gens et al. teach in figure 2 a semiconductor chip having a substrate (figure 4, the external line encircling R1) of a first conductivity type, the chip comprising: a plurality of pads P1, P2, an ESD positive line R1 not being connected to a steady voltage source, an ESD negative ring R2, and a plurality of floating lateral clamp diodes (column 3, lines 48-49) connected to the pad so that each first and second floating lateral clamp diodes is connected to the pad and the positive and negative lines, respectively.

Gens et al. do not teach a plurality of ESD protection devices, and plurality of ESD switches connected to the positive line and the negative ring, respectively.

Bass Jr. et al. teach in figure 7 teach a plurality of ESD protection devices independently connected to multiplicity of power supplies.

APA teaches in figure 1 a plurality of ESD switches connected to the positive line and to the negative ring, respectively (page 2, lines 24-27).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to independently connect a plurality of Gens et al.'s ESD

protection devices to each power supply source in an integrated circuit associated with multiplicity of isolated power supplies, in order to provide more reliable protection for the device.

It would also have been obvious to a person of ordinary skill in the art at the time the invention was made to connect plurality of ESD switches to plurality of positive lines and to the negative ring, respectively, in Gens et al.'s device, because it is conventional to connect plurality of ESD switches between plurality of positive lines and the negative ring in order to provide effective unidirectional flow of current during ESD operation.

Regarding claim 19, Gens et al. teach in figure 4 a negative line encircling the periphery of the chip.

Regarding claims 22-23, Gens et al. teach floating ESD positive and negative rings connected package pins (column 2, line 43).

Regarding claims 34 and 35, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to form the ESD switches between two adjacent corners of the chip, since the location of the switch on the chip is a matter of

design choice within the skills of an artisan, subject to routine experimentation and optimization regarding the operation of the device.

Regarding claim 36, APA teaches in figure 1 a driver transistor connected to the steady voltage line and the pad.

10. Claims 17-18 and 20-21, insofar as in compliance with 35 U.S.C. 112, are rejected under 35 U.S.C. 103(a) as being unpatentable over Gens et al., Bass Jr. et al. and APA, as applied to claim 15 above, and further in view of Rao et al.
Gens et al., APA and Bass Jr. et al. teach substantially the entire claimed structure, as applied to claim 15 above, except disclosing the structure of the floating diode.
Rao et al. teach the entire claimed structure of the floating diode of claims 17-18 and 20-21, as recited in sections 7 and 8 of the office action, respectively.
It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form the floating diodes of Gens et al. in a circular second and third region, respectively, within a double well, as taught by Rao et al., because it is well known in the art to form floating devices including diodes in a double well configuration in order to provide better electrical isolation to the devices.

11. Claims 1, 5, 6, 10, 11, 15, 17-23 and 32-36, insofar as in compliance with 35 U.S.C. 112, are rejected under 35 U.S.C. 103(a) as being unpatentable over Gens et al., Bass Jr. et al. and APA, as applied to claim 15 above, and further in view of Ker (5,744,842) and Rao et al.

Gens et al., APA and Bass Jr. et al. teach substantially the entire claimed structure, as applied to claim 15 above, except disclosing the structure of the floating diode.

Ker teaches in figure 15 substantially the entire claimed structure of the floating diode, including a well of a second conductivity type 312, a plurality of spaced apart P+ regions 300 being electrically connected together, and an N+ region 302 being formed in the well and having dopant concentration higher than that of the well (figure 14), wherein the third region encircles the first region, and an N+ region formed in the well, and having a dopant concentration higher than that of the well.

Ker does not teach an N- region formed in the well. Rao et al. further teach in figure 9 a first region of a second conductivity type 111 being formed in the well 108, and having a dopant concentration that is less than that of the well.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form the floating diodes of Gens et al. in a circular third region within a double well, as taught by Ker and Rao et al., because it is well known in the art to form floating devices including diodes in a double well configuration in order to provide better electrical isolation to the devices.

Response to Arguments

12. Applicant argues on pages 5-8 that there is support in the specification for a second region of a second conductivity type being formed in a well of a second conductivity type and encircling that particular well. Applicant recites a well, a second region of a second conductivity type being formed in the well, wherein the second region encircles that particular well ("the second region encircles the top surface of the well"). The phrase 'the well' means 'that particular well'. Although it is possible for the second region to encircle part of the well, it is impossible for the second region to be formed within the well and to encircle the whole well, at the same time. Therefore, there is no support in the specification for a second region of a second conductivity type encircling a well of a second conductivity type, as recited in claims 1 and 18.

13. Applicant argues on pages 9-11 that in rejecting claims 2-3 and 10-11, certain elements could not be found in Rao et al.'s reference. There might be some confusion regarding the rejection of claims 2-3 and 10-11, because identical elements were named differently in claims 2-3 and 10-11. For example, the P+ regions were named as first regions in claim 2, and as second regions in claim 10. The N+ regions were named as second regions in claim 3, and as third regions in claim 11. Therefore, to avoid further confusion, the present office action contains separate sections for claims 1 and 10.

14. Applicant's arguments with respect to claims 1, 5, 6, 10, 11, 15, 17-23 and 32-36 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

15. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Papers related to this application may be submitted to Technology center (TC) 2800 by facsimile transmission. Papers should be faxed to TC 2800 via the TC 2800 Fax center located in Crystal Plaza 4, room 4-C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). The Group 2811 Fax Center number is (703) 308-7722 and 308-7724. The Group 2811 Fax Center is to be used only for papers related to Group 2811 applications.

Any inquiry concerning this communication or any earlier communication from the Examiner should be directed to *Examiner Nadav* whose telephone number is **(703) 308-8138**. The Examiner is in the Office generally between the hours of 7 AM to 3 PM (Eastern Standard Time) Monday through Friday.

Any inquiry of a general nature or relating to the status of this application should be directed to the **Technology Center Receptionists** whose telephone number is **308-0956**

Tom Thomas

Ori Nadav, Ph.D.

September 29, 2000